ESTRATTA

UNIVERSITÀ DEGLI STUDI DI TRIESTE

BUSTA N. 2

A2. Effettuare la misura della caratteristica tensione corrente di un diodo con Picoamperometro Keithley 6487.

B2 Si chiede al/alla Candidato/a di progettare un setup per la caratterizzazione di un sensore di particelle a diverse temperature in camera climatica. Il candidato descriva criteri, scelte e strumentazione che intende proporre.

C2 Il/la Candidato/a illustri le funzioni del Direttore Generale come definite dallo Statuto dell'Università degli Studi di Trieste.

D2. Il/la Candidato/a legga e traduca alcune frasi dalla pagina 11, cap. 2 del manuale del modulo CAEN V775/V775N

E2 Il/la Candidato/a apra un foglio excel, inserisca due numeri in due caselle diverse, inserisca la formula per la somma di questi due numeri in un'altra casella, e salvi il file.

2. Principles of operation

The board has 32 (16 for the Mod. V775 N) channel inputs and one COM input (ECL/NIM) common to all channels. The Mod. V775 N does not feature the ECL GATE input.

The time intervals between the input and COM signals are converted into a voltage level by the TAC sections and then are multiplexed and converted by two fast 12-bit ADC modules.

Only the values that are above a programmable threshold (see § 2.4), do not cause overflow (see § 2.5) and are not killed (see § 2.4) will be stored in a dual port data memory accessible via VME.

In the following functional sections and operation principles of the module are described in some detail. The block diagram of the module can be found in Fig. 1.2.

2.1. Operating mode description

The Mod. V775 can operate either in Common Start or Common Stop mode. The operating mode can be selected via the bit 10 of the Bit set 2 register (please refer to § 4.25).

2.2. TAC sections

The module hosts 32 (16 for the Mod. V775 N) TAC (Time to Amplitude Conversion) sections; a TAC section converts the time interval between Start and Stop signals to a proportional voltage level (a simplified block diagram is reported in Fig. 2.1). A Start signal closes the switch SW1 thus allowing a constant current to flow through an integrator; a Stop signal opens the switch SW1 again. The constant current generates a linear ramp voltage which is stopped at an amplitude proportional to the time interval between Start and Stop pulses. After digitisation the SW2 switch is closed by the CLEAR signal which allows the discharge of the capacitor C1. Both the COMMON and CLEAR signals are controlled by the CONTROL LOGIC section. The timing of signals during data acquisition is shown in Fig. 2.2.

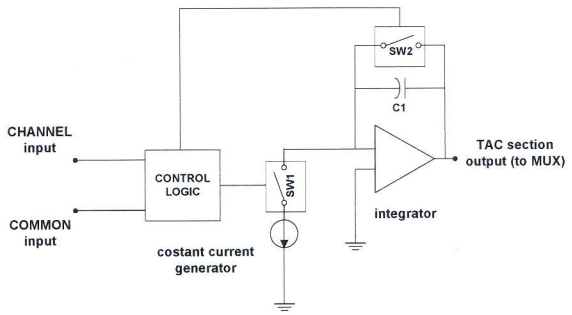

Fig. 2.1: Simplified block diagram of the TAC section