NON ESTRATTA

UNIVERSITÀ DEGLI STUDI DI TRIESTE

BUSTA N. 4

A4. Misurare con un oscilloscopio le caratteristiche tipiche di un segnale analogico. Fornire questo segnale in ingresso ad un modulo CAEN N844 per ottenere un segnale logico.

B4 Si chiede al/alla Candidato/a di progettare un setup per polarizzare inversamente un diodo e monitorarne la corrente ad intervalli regolari per un certo periodo di tempo. Il candidato descriva criteri, scelte e strumentazione che intende proporre.

C4 Il/la Candidato/a illustri le funzioni del Senato Accademico come definite dallo Statuto dell'Università degli Studi di Trieste.

D4. Il/la Candidato/a legga e traduca alcune frasi dalla pagina 15, par. 2.5 del manuale del modulo CAEN V775/V775N

E4 Il/la Candidato/a apra un foglio excel, inserisca due numeri in due caselle diverse, inserisca la formula per il prodotto di questi due numeri in un'altra casella, e salvi il file.

If the result of the comparison is true and the Bit 4 (LOW THRESHOLD PROG) of the Bit Set 2 Register is set to 0, data are skipped. If the Bit 4 of the Bit Set 2 Register is set to 1, the true result of the comparison is signalled by Bit 13 (UNDERTHRESHOLD) = 1 in the loaded data 16 bit word.

The content of the Threshold Register includes also a KILL bit, which allows to abort the memorisation of the datum even if it is higher than the threshold set in the register. This bit can thus be used to disable some channels. Refer to § 4.39 for further details.

The threshold values are lost only after switching the board off (a reset operation does not affect the threshold values).

2.5. Overflow suppression

The overflow suppression allows to abort the memorisation of data which originated an ADC overflow. The control logic provides to check if the output of the ADC is in overflow and, in the case, the value is not stored in the memory.

The overflow suppression can be disabled by means of the OVER RANGE PROG bit of the Bit Set 2 Register (see § 4.25): if this bit is set to 1, all the data, independently from the fact that they caused ADC overflow or not, are stored in the memory. In this case, the 16-bit word stored in the memory will have the bit 12 (OVERFLOW) set to 1 (see § 4.5)

2.6. Not valid data suppression

When the module works in Common Stop mode, it may occur that a TAC output saturates before the arrival of a Stop signal; in this case the TAC section resets itself through constant current capacitor discharge and after approximately 700 ns the channel is ready to accept a new Start signal. If a Stop signal arrives when the TAC is resetting the datum is not valid (this condition is flagged by the bit 14 of the data word (see § 4.5)).

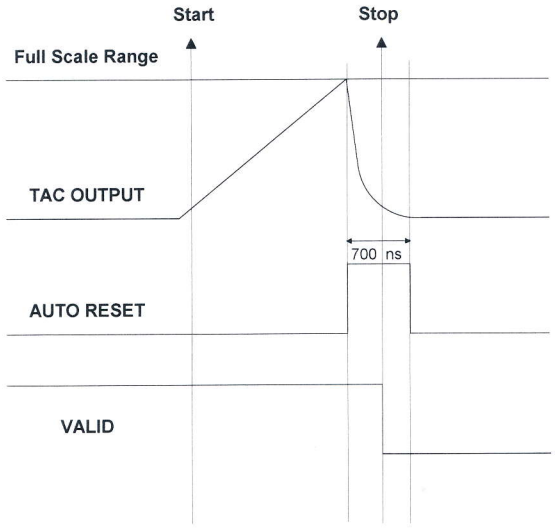

Fig. 2.6: TAC autoreset in Common Stop mode